Abstract of the Disclosure

A data output circuit includes a plurality of registers and a plurality of register output selection switches that are respectively connected to the plurality of registers. Pairs of the plurality of register output selection switches are connected by respective common active regions. A first data group selection switch is connected to the common active regions of a first set of the plurality of register output selection switches. A second data group selection switch is connected to the common active regions of a second subset of the plurality of register output selection switches. An output driver is connected to the first and second data group selection switches.